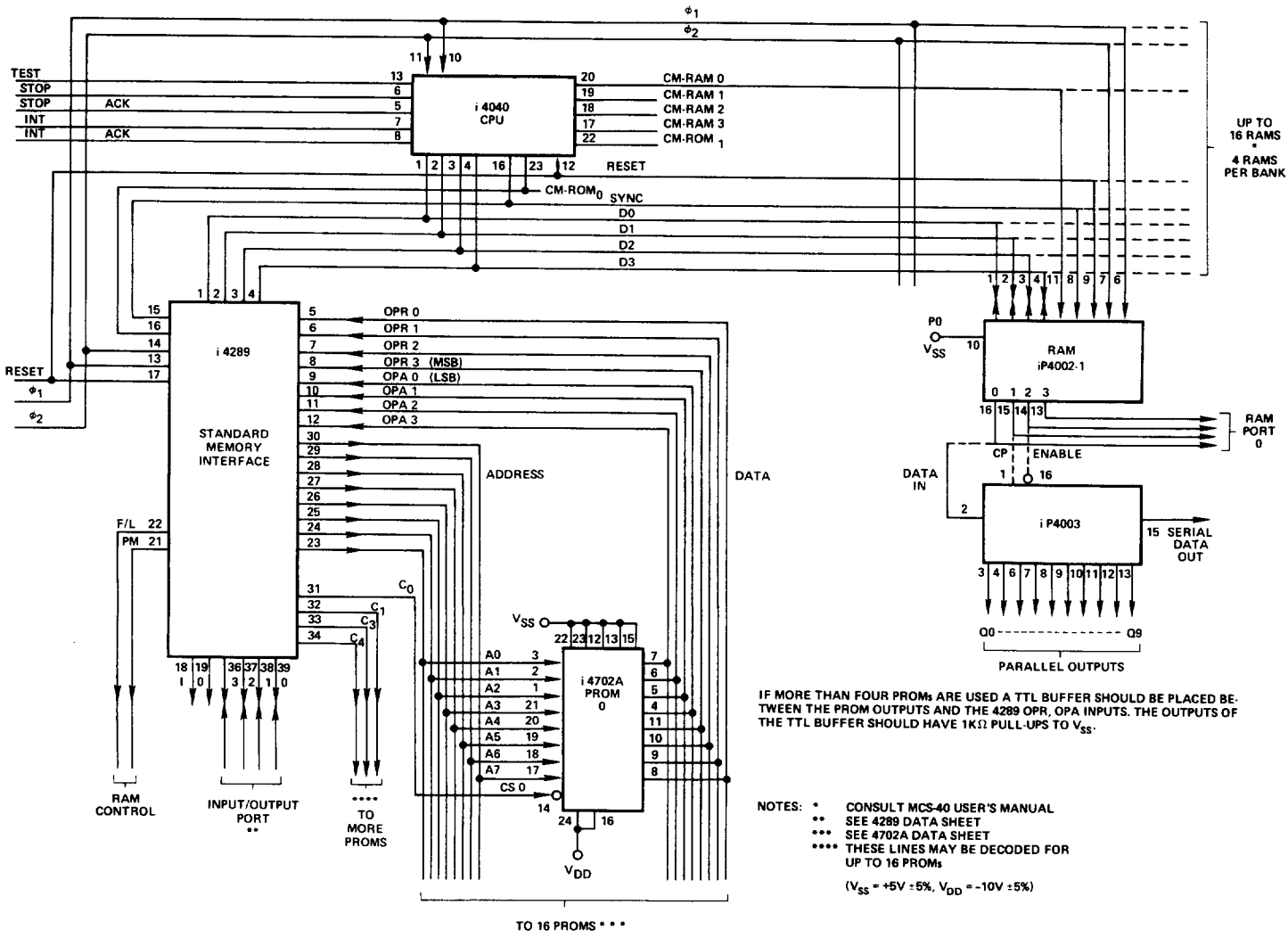
SYSTEM INTERCONNECT

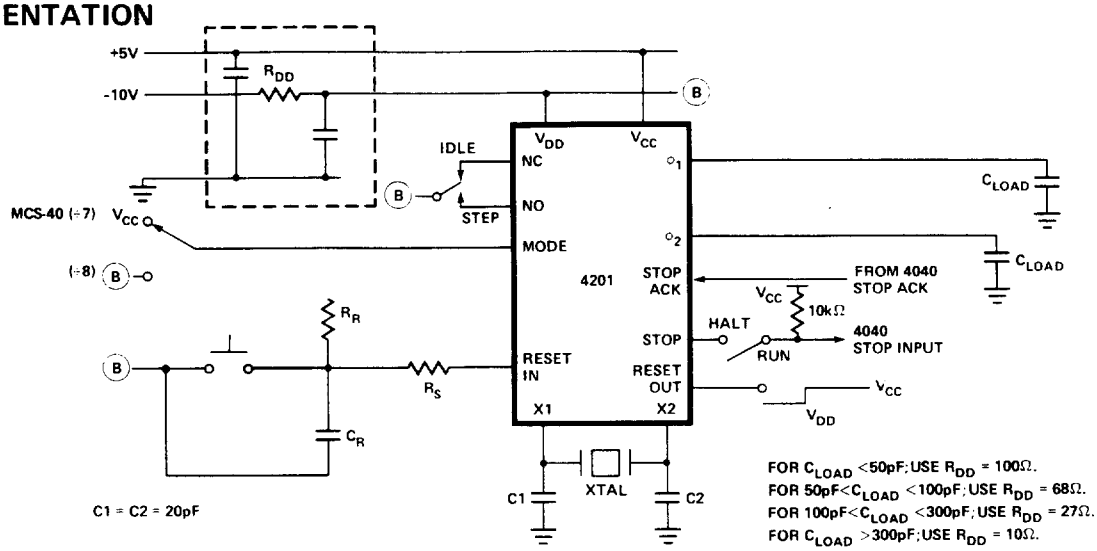


IF MORE THAN FOUR PROMs ARE USED A TTL BUFFER SHOULD BE PLACED BETWEEN THE PROM OUTPUTS AND THE 4289 OPR, OPA INPUTS. THE OUTPUTS OF THE TTL BUFFER SHOULD HAVE 1KΩ PULL-UPS TO V_{SS}.

NOTES:
- * CONSULT MCS-40 USER'S MANUAL
- ** SEE 4289 DATA SHEET
- *** SEE 4702A DATA SHEET
- **** THESE LINES MAY BE DECODED FOR UP TO 16 PROMs

(V_{SS} = +5V ±5%, V_{DD} = -10V ±5%)

4201 IMPLEMENTATION



Operation is guaranteed with V_{CC}-V_{DD} = 15V ±5%. During system power-up or during power supply glitching, the maximum magnitude of (V_{CC}-V_{DD}) must be limited to 17 volts.

With V_{CC} = +5V, V_{DD} = -10V, bypass capacitors of 1 μF and .1 μF in parallel from V_{CC} to GND and also V_{DD} to GND provide excellent bypassing.

The purpose of R_{DD} is both to limit ϕ_1 and ϕ_2 rise times and to drop V_{DD} at the 4201 pin. Values for R_{DD} are specified below.

The XTAL terminals, X1 and X2, should each be tied to a 20 pF capacitor to GND. The same value should be used on both X1 and X2.

Either ÷7 or ÷8 Modes may be used. Mode equals V_{CC} for ÷7, Mode equals V_{DD} for ÷8. Refer to MCS-40™ User's Manual.

The Reset input has V_{IL} = V_{CC} -11 Volts and V_{IH} = V_{CC} -6.5 Volts, with about 1 Volt of hysteresis (Schmitt circuit). Node (A) must be tied to GND or V_{CC} = +5V; and R_R and C_R selected, such that the negative V_{DD} transition moves the Reset input below V_{IL}.

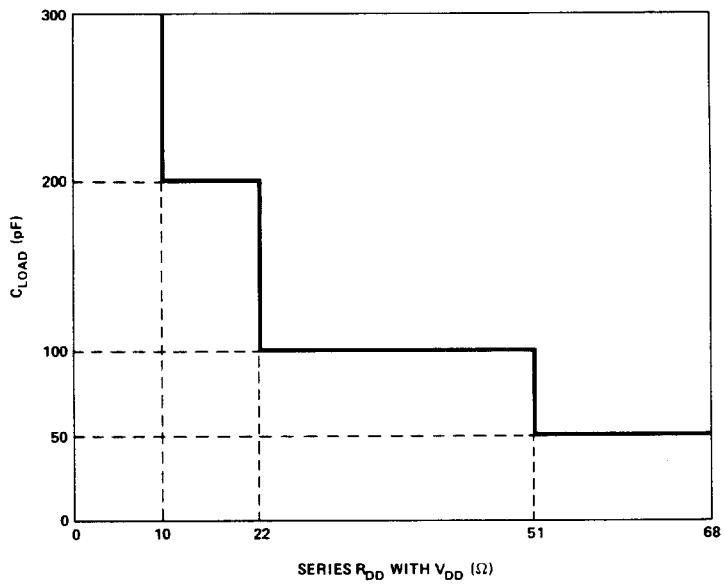
Tying node (A) to GND and making C_R very large, i.e. >1 μF, will allow the greatest freedom in V_{CC} and V_{DD} rise times during turn-on. Tying node (A) to GND will also cause Reset after a V_{DD} glitch to GND.

The purpose of R_S. at 510Ω or 1kΩ, is to limit Reset input fall time on manual Reset, so that the Reset input does not fall below V_{DD}.

The XTAL range should be between 500 kHz (4 MHz XTAL, ÷8 MODE) and 740 kHz (5.185 MHz XTAL, ÷7 MODE). These XTAL may be found as standard product from CTS Knight or Crystek.

GND pin may be tied to V_{CC} if ϕ_{1T} and ϕ_{2T} are not used; if ϕ_{1T} and ϕ_{2T} are used, GND pin should be tied to logic ground. ϕ_{1T} and ϕ_{2T} levels will be equal to V_{CC} and the GND pin level.

RESISTOR R_{DD} VS. ϕ_1, ϕ_2 LOAD CAPACITANCE



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MCS-40™ PROTOTYPE SYSTEM

MCS-40 SYSTEM A

MCS-40 SYSTEM—INTEL'S LOWEST COST MICROCOMPUTER. IDEAL FOR PROTOTYPE OR LOW VOLUME PRODUCTION AND RANDOM LOGIC REPLACEMENT.

The MCS-40 Microcomputer gives the user the design and computational capability of larger and more complex computers with just a small assortment of easy to use components. The set of parts are designed to offer the user an economical alternative to random logic.

The basic kit consists of the following standard building blocks:

- 4040 CPU
- 4289 Standard Memory Interfaces with I/O
- 4002 RAM with output
- 4003 Shift Register
- 4702A Programmable ROM
- 4201 System Clock

Due to the high degree of modularity of the MCS-40 system, additional components can be added to the kit to optimize it for the user's unique application. All components are fabricated with silicon gate, low threshold, PMOS technology.

The MCS-40 systems interface easily with switches, keyboards, displays, printers, communication terminals, and other popular peripherals.

A system built with the MCS-40 microcomputer set can have up to 8K x 8 of program memory in ROM or PROM, 1280 x 4-bit of RAM data memory and over 128 I/O lines, without requiring any interface logic. Further expansion of this very powerful system is accomplished with the addition of a few simple gates.

The MCS-40 Microcomputer has a very extensive instruction set which designers find extremely easy to use. The instruction set includes 60 powerful instructions, including true interrupt and a single step mode of operation. The basic instruction set consists of:

- Binary and Decimal Arithmetic
- Logical AND and OR
- Add and Subtract from Memory
- Rotate, Complement, and Test Accumulator
- Increment Registers
- Exchange Registers with Accumulator
- Conditional and Unconditional Branches and Subroutine Calls
- Increment, Test, and Branch in Single Instructions
- I/O Instructions
- Special Keyboard Instruction
- Interrupt Enable/Disable
- ROM and Register Bank Switching

In addition to the large assortment of MCS-40 components, Intel offers a complete line of resident and cross software products, hardware development aids such as the Intellec 4/MOD 40 development system, user field training courses and an extensive staff of field application engineers to assist you with your unique design.

Programmable General Purpose Microcomputer

Program Storage in 4702A Reprogrammable PROM Simulates ROM

Large number of family devices

10.8 microsecond instruction cycle

2-phase dynamic operation

Instruction set (60 total) includes conditional branching, jump to subroutine and indirect fetching

Logical instructions

Binary and decimal arithmetic modes

CPU directly compatible with MCS-4 ROMs and RAMs

Unlimited number of input and output lines

Interrupt capability

Single step operation

8K byte memory addressing capability and up to 5120 bits of RAM

24 index registers

Subroutine nesting to 7 levels